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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/039,587 | 12/31/2001 | Steven J. Tu | 42390P12013 | 2260 |

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| EXAMINER | |
|---|---|
| CHAUDRY, MUJTABA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/039,587 | TU ET AL. | |
| | Examiner | Art Unit | |
| | Mujtaba K. Chaudry | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

The corrected or substitute drawings were received on February 28, 2005. These drawings are accepted.

### *Specification*

The corrected or substitute specification were received on February 28, 2005. The specification is accepted.

### *Response to Amendment*

Applicant's arguments/amendments with respect to amended claims 2-6 and 8 and original claims 1, 7 and 9-20 filed February 28, 2005 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...the references '366 and 756 (prior arts of record) do not teach or suggest a timer to trigger an FRC recovery routine if the status indicates the results do not match and the error check unit does not assert the signal within a specified interval..." The Examiner respectfully disagrees. The timer in the present application is used to trigger the FRC recovery unit when the results do not match and the error check unit fails. The '366 reference teaches (col. 4, lines 50-68) the execution mode of the processor as a whole may be tracked through a single processor status bit. The mode can be triggered from HP to HR which is analogous to triggering the FRC recovery routine in the present application. The Examiner would like to point out that

although the reference '366 does not explicitly teach to switch the modes based on a timer, the timer limitation is not patentably distinguishing from the prior arts of record. This would be any obvious engineering design modification which is well know in the art.

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 2-6 and 8 and original claims 1, 7 and 9-20. All arguments have been considered. It is the Examiner's conclusion that amended claims 2-6 and 8 and original claims 1, 7 and 9-20, as presented, are not patentably distinct or non-obvious over the prior art of record. See office action:

***Claim Rejections - 35 USC § 103***

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grochowski et al. (USPN 6615366B1) further in view of Grochowski et al. (USPN 6625756).

As per claims 1, 9 and 17, Grochowski et al. (USPN 6615366B1, herein after: Reference '366) substantially teaches (title and abstract) a microprocessor with dual execution cores that may be switched between high reliability and high performance execution modes dynamically,

according to the type of code segment to be executed. When the processor is in high performance mode, the dual execution cores operate in lock step on identical instructions, and the execution results generated by each execution core are compared to detect any errors. In high performance monde, the dual execution cores operate independently. Reference '366 teaches (col. 1, lines 11-68) one way of detecting soft errors in an execution core is to process instructions on duplicate execution cores and compare results determined by each on an instruction by instruction basis ("redundant execution"). For example, one computer system includes two separate processors that may be booted to run in either a symmetric multi-processing ("SMP") mode or a Functional Redundant Check unit ("FRC") mode. In SMP mode, instruction execution is distributed between the processors to provide higher overall performance than single processor systems. In FRC mode, the processors execute identical code segments and compare their results on an instruction by instruction basis to determine whether an error has occurred. The operating mode can only be switched between SMP and FRC modes by resetting the computer system. Another computer system provides execution redundancy using dual execution cores on a single processor chip. This approach eliminates the need for inter-processor signaling, and detected soft errors can usually be corrected. Reference '366 teaches (Figure 2A) each execution core 110 is represented as a series of stages in an instruction execution pipeline. Each stage corresponds to one or more operations implemented by execution cores 110 to execute their instructions. Alternatively, the pipeline stages may be understood to represent the logic that executes the indicated operations. Instructions and data are provided to execution cores 110 from a memory system 270. Cache 280 represents a portion of memory system 270 to which results from executed instructions are written. Cache 280 may be located on the same

chip as processor 100 or it may be located on a separate chip. Each execution core 110 is partitioned into a fetch (FET) stage 210, a decode (DEC) stage 220, register (REG) stage 230, an execute (EXE) stage 240, a detect (DET) stage 250, and a retirement (RET) stage 260. One or more instructions are retrieved from memory system 270 in FET stage 210. The retrieved instructions are decoded at stage 220, and source operands are retrieved in REG stage 230.

Reference '366 does not explicitly teach a timer to trigger an FRC recovery routine if the status indicates the results do not match as stated in the present application.

However, Grochowski et al. (USPN 6625756B1, herein after: Reference '756) teaches, in an analogous art, (title and abstract) a processor is provided that implements a replay mechanism to recover from soft errors. The processor includes a protected execution unit, a check unit to detect errors in results generated by the protected execution unit, and a replay unit to track selected instructions issued to the protected execution unit. When the check unit detects an error, it triggers the replay unit to reissue the selected instructions to the protected execution unit. One embodiment of the replay unit provides an instruction buffer that includes pointers to track issue and retirement status of in-flight instructions. When the check unit indicates an error, the replay unit resets a pointer to reissue the instruction for which the error was detected. Reference '756 teaches the Replay unit 170 to track selected instructions in protected execution unit 180 until they are retired. When an instruction is retired, results generated by the instruction update the architectural state of the processor ("processor state"). For this reason, it is important to detect and correct soft errors before the instructions that are affected by the soft error retire. Since soft errors are a product of transient phenomena (cosmic rays, alpha particles), data corruption attributable to these errors can frequently be eliminated by re-executing instructions that are

affected by the soft error. For example, soft errors that corrupt data in execution, control, and delivery circuits are unlikely to recur when instructions are re-executed. These soft errors may be addressed by re-executing selected instructions beginning with the instruction for which the soft error was first detected. Soft errors may also corrupt data in various storage structures associated with the execution resources. Re-executing instructions that merely retrieve corrupted data does not eliminate the problem. However, the corrupted data may be restored by various hardware and software mechanisms, e.g. ECC hardware or firmware. These soft errors may be addressed by re-executing the instructions once the data has been recovered data. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a timer to trigger the FRC recovery unit if the status indicates that the results from the two cores do not match within the method and apparatus of Reference '366. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by incorporating a timer to trigger the FRC recovery unit if the status indicates that the results from the two cores do not match would have increased the synchronization of the two cores.

As per claims 2-5, 11-12 and 18-20, Reference '366 teaches, in view of above rejections, (col. 5) processor 100 may include a buffer to decouple front-end stage(s) from back-end stages. The buffer temporarily stores fetched (or fetched and decoded) instructions. This allows front-end operations to continue, even if back-end operations are stalled or otherwise delayed. It also allows back-end operations to proceed if front-end operations are delayed. Embodiments of processor 100 may also employ a decoupling buffer to correct errors detected in HR mode. The processor 100 does not have to be partitioned into a particular set of pipeline stages. For

example, a disclosed stage may be subdivided into two or more stages to address timing issues or facilitate higher processor clock speeds. Alternatively, two or more stages may be combined into a single stage. The disclosed pipeline provides only one example of how operations may be partitioned in a processor. Also shown for each execution core 110 is status/control (S/C) registers 234, data registers 238, and a data cache 244. S/C registers 234 store information that governs the operation of execution core 110. For example, S/C registers 234 typically include CSR 120 (and CSB 124). Data registers 238 store operands for use by various resources in execution core 110, and data cache 244 buffers operands between memory system 270 and other resources in execution core 110. Depending on timing constraints, data cache 244 may provide operands to data registers 238 or directly to execution resources in EXE stage 240. Execution cores 110(a) and 110(b) are synchronized to operate on identical instructions in lock step when processor 100 is in HR mode. In HP mode, execution cores 110(a) and 110(b) operate on different instructions. As noted above, various embodiments of processor 100 may support different levels of coordination between execution cores 110(a) and 110(b) in HP mode, as indicated by the dashed arrow in FIG. 2A. For example, if processor 100 operates as a single chip SMP system in HP mode, the need for coordination between execution cores 110(a) and 110(b) arises mainly during mode switches. For other embodiments of processor 100, execution cores 110(a) and 110(b) may handle processes that are closely coupled. These embodiments support some sharing of data between S/C registers 234(a) and 234(b), data registers 238(a) and 238(b), and data caches 244(a) and 244(b), as well as some coordination of operations between the different pipe stages.

As per claims 6-8 and 10, Reference '366 teaches, in view of above rejections, (Figure 1) the processor 100 at a later time when IA_8 and S_HR have reached the RET stages of execution cores 110(a) and 110(b), respectively, and an S_HR instruction has entered execution core 110(a). The number of clock cycles between S_HR instructions in execution cores 110(a) and 110(b) depends on the scheduling mechanism employed and the state of the currently executing HP processes when the HR thread is ready for execution. For example, IA_9 may involve a relatively long latency I/O operation that provides a natural breaking point in the thread A instruction flow. The instruction flow of thread A may be suspended when IA_9 is detected, and S_HR may be inserted following IA_9. Alternatively, IA_9 may be the last instruction in process A. Different embodiments of processor 100 may or may not continue to fetch instructions into execution cores 110 following S_HR instructions and prior to the switch to HR mode. Instructions that enter execution core 110(a) after the S_HR instruction but before processor 100 switches to HR mode are flushed when S_HR retires. These instructions are re-executed at a later time. In FIG. 4B, instructions following S_HR instructions are shown with dashed lines to indicate that they will not be retired. For example, these may represent the first instructions of the HR process thread that will be flushed and re-executed once the other execution core is synchronized. Alternatively, FET may inject NOPs into execution core 110(a) until the mode switch is complete.

As per claims 13-16, Reference '756 teaches, in view of above rejections, (Figure 2A) a processor is that implements a replay mechanism to recover from soft errors. The processor includes a protected execution unit, a check unit to detect errors in results generated by the protected execution unit, and a replay unit to track selected instructions issued to the protected

execution unit. When the check unit detects an error, it triggers the replay unit to reissue the selected instructions to the protected execution unit. The replay unit provides an instruction buffer that includes pointers to track issue and retirement status of in-flight instructions. When the check unit indicates an error, the replay unit resets a pointer to reissue the instruction for which the error was detected.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
May 19, 2005

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